IN THE CLAIMS:

The following is a complete listing of the claims in this application, reflects all changes currently being made to the claims, and replaces all earlier versions and all earlier listings of the claims:

1.-22. (Canceled)

23. (Currently Amended) An image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements;

a plurality of output lines which output, in parallel at the same time, signals of all of the photo-detection elements included in the block; and

an operation section which inputs, in parallel, the signals outputted in parallel from said plurality of output lines, wherein said operation section performs an interpolation processing to interpolate a predetermined signal using signals other than the predetermined signal.

24. (Previously Presented) An image pickup element according to claim 23, wherein said pixel area includes a plurality of partial pixel-areas arranged two-dimensionally in horizontal and vertical directions, and wherein each of the plurality of partial pixel-areas includes photodetectors arranged two-dimensionally in the horizontal and vertical directions,

wherein said image pickup element further comprises a memory which stores signals of a plurality of lines of the photodetectors arranged in the horizontal direction, and a selecting circuit which reads out the signals in parallel from the memory to said plurality of output lines on a partial pixel-area basis.

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25. (Currently Amended) An image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements;

a plurality of output lines which output, in parallel at the same time, signals of all of the photo-detection elements included in the block; and

an operation section which inputs, in parallel, the signals outputted in parallel from said plurality of output lines, wherein said operation section performs a compression processing.

26. (Previously Presented) An image pickup element according to claim 25, wherein said pixel area includes a plurality of partial pixel-areas arranged two-dimensionally in horizontal and vertical directions, and wherein each of the plurality of partial pixel-areas includes photodetectors arranged two-dimensionally in the horizontal and vertical directions,

wherein said image pickup element further comprises a memory which stores signals of a plurality of lines of the photodetectors arranged in the horizontal direction, and a selecting circuit which reads out the signals in parallel from the memory to said plurality of output lines on a partial pixel-area basis.

27. (Previously Presented) An image pickup element according to claim 25, wherein the compression processing includes a discrete cosine transform.

28. (Currently Amended) An image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements;

a plurality of output lines which output, in parallel at the same time, signals of all of the photo-detection elements included in the block; and

an operation section which inputs, in parallel, signals originating from the signals outputted in parallel from said plurality of output lines, wherein said operation section performs edge-emphasis processing.

29. (Previously Presented) An image pickup element according to claim 28, wherein said pixel area includes a plurality of partial pixel-areas arranged two-dimensionally in horizontal and vertical directions,

wherein each of the plurality of partial pixel-areas includes photodetectors arranged two-dimensionally in the horizontal and vertical directions, and

wherein said image pickup element further comprises a memory which stores signals of a plurality of lines of the photodetectors arranged in the horizontal direction, and a selecting circuit which reads out the signals, in parallel, from the memory to said plurality of output lines on a partial pixel-area basis.